AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions, and listings, of claims:

1. (Original) A method, comprising:

providing a semiconductor substrate;

forming electrically conductive columns on the semiconductor substrate;

forming electrically conductive rows crossing over the electrically conductive columns;

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and

forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column.

2. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on a thickness of electrically resistive material that forms an individual memory component.

3. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on an area of electrically resistive material that forms an individual memory component.

4. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on a geometric shape of electrically resistive material that forms an individual memory component.

5. (Original) A method as recited in claim 1, wherein the plurality of memory components are each formed to have a different resistance value based on a different area of electrically resistive material that forms a memory component.

6. (Original) A method as recited in claim 1, wherein the plurality of memory components are each formed to have a resistance value based on a rectangular geometric shape of electrically resistive material that forms a memory component, at least some of the rectangular geometric shapes having different resistance values corresponding to an area of a rectangular geometric shape.

7. (Original) A method as recited in claim 1, wherein forming the non-volatile memory cells comprises:

forming a first memory cell having a memory component that indicates logical bits 00 (zero-zero);

forming a second memory cell having a memory component that indicates logical bits 01 (zero-one);

forming a third memory cell having a memory component that indicates logical bits 10 (one-zero); and

forming a fourth memory cell having a memory component that indicates logical bits 11 (one-one).

8. (Original) A method as recited in claim 1, wherein forming the non-volatile memory cells comprises:

forming a first memory cell that indicates logical bits 00 (zero-zero) corresponding to a first resistance value based on an area of electrically resistive material that forms a memory component in the first memory cell;

forming a second memory cell that indicates logical bits 01 (zero-one) corresponding to a second resistance value based on an area of electrically resistive material that forms a memory component in the second memory cell;

forming a third memory cell that indicates logical bits 10 (one-zero) corresponding to a third resistance value based on an area of electrically resistive material that forms a memory component in the third memory cell; and

forming a fourth memory cell that indicates logical bits 11 (one-one) corresponding to a fourth resistance value based on an area of electrically resistive material that forms a memory component in the fourth memory cell.

9. (Original) A method as recited in claim 1, wherein forming the plurality of memory components comprises forming individual memory components with a resistor in series with a diode.

10. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing the memory component to light.

11. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing electrically resistive material forming the memory component to light.

12. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing the memory component to heat.

13. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing electrically resistive material forming the memory component to heat.

14. (Original) A method as recited in claim 1, wherein forming the non-volatile memory cells comprises:

forming a first non-volatile memory cell by connecting a first memory component between an electrically conductive row and a first electrically conductive column, the first non-volatile memory cell formed as part of a first layer of non-volatile memory cells; and

forming a second non-volatile memory cell by connecting a second memory component between the electrically conductive row and a second electrically conductive column, the second non-volatile memory cell formed as part of a second layer of non-volatile memory cells.

15. (Withdrawn) A method of making a non-volatile read-only memory device, comprising:

providing a semiconductor substrate;

forming a first layer on the semiconductor substrate;

forming one or more additional layers over the first layer;

wherein forming an individual layer comprises:

forming a plurality of conductive traces; and

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits where each memory component is connected between a first conductive trace and a second conductive trace.

16. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, wherein the plurality of memory components are each formed to have a resistance value based on a thickness of electrically resistive material that forms a memory component.

17. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, wherein the plurality of memory components are each formed to have a resistance value based on an area of electrically resistive material that forms a memory component.

18. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, wherein the plurality of memory components each have a resistance value based on a geometric shape of electrically resistive material that forms a memory component, at least some of the geometric shapes having different resistance values corresponding to an area of the geometric shapes.

19. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, wherein forming the plurality of memory components comprises:

forming a first memory component having a resistance value corresponding to logical bits 00 (zero-zero);

forming a second memory component having a resistance value corresponding to logical bits 01 (zero-one);

forming a third memory component having a resistance value corresponding to logical bits 10 (one-zero); and

forming a fourth memory component having a resistance value corresponding to logical bits 11 (one-one).

20. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, wherein forming the plurality of memory components comprises forming individual memory components with a resistor in series with a diode.

21. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, further comprising configuring the resistance value of individual memory components by exposing a memory component to light.

22. (Withdrawn) A method of making a non-volatile read-only memory device as recited in claim 15, further comprising configuring the resistance value of individual memory components by exposing a memory component to heat.